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TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

In re application of:	Stephen Melvin Mario D. Nemirovsky
Serial No.:	09/592106
Filed:	06/12/00
Docket:	MIPS.0167-00-US
For:	METHOD AND APPARATUS FOR IMPLEMENTING ATOMICITY OF MEMORY OPERATIONS IN DYNAMIC MULTI-STREAMING PROCESSORS

Attached hereto is Form PTO-1449 listing documents believed relevant to the subject application. It is respectfully requested that the Examiner review the information disclosed herein in detail, independently evaluate each item carefully in the consideration of the pending claims and return an initialed copy of each form to the undersigned.

This disclosure statement should not be construed as a representation that a search has been made, that no other material information as defined in 37 C.F.R. § 1.56(a) exists, or as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b) or is available as a reference under 35 U.S.C. § 102 *et seq.* Applicant reserves the right to swear behind or otherwise disprove the alleged "prior" nature of any art cited should the facts support and the situation warrant such an action.

It is believed that this disclosure complies with the requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98, and the Manual of Patent Examining Procedures § 609. If for some reason the examiner considers otherwise, it is respectfully requested that the undersigned be called so that any deficiencies can be remedied.

A copy of each document is enclosed. Some of the documents may have markings thereon. No significance is intended to be attached to the markings.

Respectfully submitted,

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"EXPRESS MAIL" mailing label number EO003677317US
Date of Deposit 1-4-05. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Alexandria, VA 22313.
By: Nicki J. Hoy

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary

Sheet	1	of	2

Complete if Known	
Application Number	09/592106
Filing Date	06/12/00
First Named Inventor	Stephen Melvin Mario D. Nemirovsky
Group Art Unit	2154
Examiner Name	Larry Donaghue
Attorney Docket Number	MIPS.0167-00-US

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	AA	DIEFENDORFF, KEITH, "WinChip 4 Thumbs Nose at ILP," *Microprocessor Report*, Vol, 12, No.16, 10 pages (December 7, 1998)	
	AB	EGGERS ET AL, "Simultaneous Multithreading: A Platform for Next-Generation Processors", IEEE Micro, 1997.	
	AC	DIEFENDORFF, KEITH; "Jalapeno Powers Cyrix's M3", Microprocessor Report, Vo. 12, No. 15, Nov. 16, 1998.	
	AD	BECKER ET AL; "The PowerPC 601 Microprocessor", IEEE Micro, IEEE 1993.	
	AE	SLATER, MICHAEL, "Rise Joins x86 Fray With mP6" Microprocessor Report, Vol. 12, No. 15, Nov. 16, 1998.	
	AF	DIEFENDORFF, KEITH; "Compaq Chooses SMT for Alpha", Microprocessor Report, Dec. 6, 1999.	
	AG	POTEL, M.J., "Real-time Playback in Animation Systems", Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp.72-77, San Jose, CA.	
	AH	ARM Architecture Reference Manual, 1996, pp.3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall.	
	AI	MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp.10-66, 10-67, and 10-71, Motorola, Inc.	
	AJ	DIFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEEE Micro, April 1992, pp.40-63, Vol. 12, No.2.	
	AK	KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp.7-106 and 7-107, Prentice hall, New Jersey.	
	AL	DIEFENDORFF, KEITH et al., "AltiVec Extension to PowerPC Accelerates Media Processing", March – April 2000, pp.85-95, IEEE Micro, Vol. 20, No.2.	
	AM	FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp.210-211, IEEE.	
	AN	YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of CA, Santa Barbara dissertation, December 1995, Santa Barbara, CA.	
	AO	STEERE et al, "A Feedback-Driven Proportion Allocator for Real Estate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp.145-158, USENIX Association.	

Examiner Signature		Date Considered	

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Sheet 2 of 2

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Examiner Name	Larry Donaghue
Attorney Docket Number	MIPS.0167-00-US

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	AP	YAMAMOTO, WAYNE, et al., "Increasing Superscalar Performance Through Multistreaming", 1995.	
	AQ	TULLSEN, DEAN, et al., "Simultaneous Multithreading: Maximizing on-Chip Parallelism", 22nd Annual International Symposium on Computer Architecture, June 1995, Santa Margherita, Ligure, Italy.	
	AR	YOAZ et al., "Speculation Techniques for Improving Load Related Instruction Scheduling", 1999, pp.42-53. IEEE.	
	AS	KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of –Order Execution at 600 Mhz", August 1998.	
	AT	"ESA/390 Principles of Operation" Table of Contents. 09/23/03; http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOKS/DZ9AR001/CCONTENTS.	
	AU	NEMIROVSKY, MARIO D. et al; "DISC: DYNAMIC INSTRUCTION STREAM COMPUTER", 1191; pp.163-171.	
	AV	NEMIROVSKY, MARIO D., "DISC, A DYNAMIC INSTRUCTION STREAM COMPUTER", September 1990.	
	AW	YAMAMOTO, WAYNE et al; "Performance Estimation of Multistreamed, Superscaler Processors", 1994 IEEE, pp. 195-204.	

Examiner Signature		Date Considered	